REMARKS

Claims 1-20 were pending in the above identified application. With this response, Claims 1 and 16 have been cancelled; Claims 3 and 19 have been rewritten in independent form, and Claims 2, 5-8, 10, 11, 13, 14, 17, 18, and 20 have been amended. Applicants respectfully request allowance of the Claims, as amended, and in light of the following.

Claim Rejections under 35 U.S.C. §102(b)

Claims 1, 6, 11, 14, 16, and 17 were rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5, 410, 451 (Hawthorne et al.). Applicants respectfully traverse the rejections.

Claims 1 and 16 have been canceled thereby rendering moot any rejection of these claims.

Independent Claim 14 has been amended to recite, in pertinent part, "the metal layer on the backside of the semiconductor chip strengthens adhesion between the semiconductor chip and the solder film." Hawthorne et al. does not disclose such limitation. As such, Claim 14 is further distinguished from Hawthorne et al. and should be allowed for at least that reason as well as the reasons recited with respect to amended Claim 3 below.

Claims 6 and 11 depend from amended Claim 3, and should be allowable at least by virtue of their dependency.

Claim 17 depends from Claim 19, which as discussed below should be in condition for allowance.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102.

Claim Rejections under 35 U.S.C. §103(a)

Claims 3, 5, 8, 9, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hawthorne et al., in further in view of US Patent No. 5,811,317 (Maheshwari et al.). Claims 2 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hawthorne et al. in view of U.S. Patent No. 5,359,768 (Haley). Applicants respectfully traverse the rejection.

Applicants have rewritten Claim 3 in independent form. Independent Claim 3 recites, in pertinent part, "a solder film directly attached to the heat slug thereby bonding the heat slug to the backside of the semiconductor chip, wherein the backside of the semiconductor chip includes a metal layer formed thereon for strengthening adhesion between the semiconductor chip and the solder film." Hawthorne et al. discloses a tape automated bonding package incorporating a die and a substrate provided with a relatively strong heat spreader/support member secured by an adhesive to one side of the die and extending to side portions of the substrate. Hawthorne et al.'s chip on tape configuration discloses one side of a die connected to free leads and the other to a heat spreader supported by a substrate below. See Hawthorne et al. Abstract, lines 5-16. Maheshwari et al., however, discloses a balance plate which "causes the die to warp to the other side and as a result the two self opposing warpage effects neutralize themselves." See Maheshwari et al. Abstract lines 9-11. Hawthorne et al. and

Maheshwari et al. teach away from combination with one another because Hawthorne et al. discloses no flexible substrate coupled directly to the bottom of the die from which the balance plate would counteract the force and minimize warpage. See Hawthorne et al. Col. 3 lines 62-64 and Fig 3. With free leads directly coupled to the bottom of the die, adding Maheshwari et al.'s balancing plate may simply put unwanted warping force on the die from the opposite direction. See Hawthorne et al., col. 3 lines 62-64 and Fig. 3. Therefore, Hawthorne et al. teaches away from adding a metal layer to the backside of a semiconductor chip as taught by Maheshwari et al. in order to minimize substrate and die warpage induced after underfill cure operations.

Claims 2, 5, 8, 9, and 13 depend from Claim 3 and are allowable for at least that reason.

Furthermore, Claims 2 and 13 should be allowable for at least the reason that there is no motivation to combine the cited references. Indeed, the references teach away from such combination. Haley discloses a package including a substrate or die coupled to a heat sink; the heat sink is coupled to the die using an adhesive, and then the die is mounted to the circuit board. Examiner states in Office Action mailed February 28, 2002, that "Haley discloses the material of the solder film (column 3, lines 66-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hawthorne et al. by selecting from a group consisting of Pb, Sn, Ag, In, and Bi for the material of the solder film as taught by Haley." Haley discloses tin and lead, however, only for its conductive solder bumps. See Col. 3 lines 66-67. These distinct solder bumps serve a function of mechanically and electrically linking with specific pads on the circuit board during the flip chip mounting process. See Col. 3 lines 23-24; Col. 1 lines 48-62; Fig. 1. Haley clearly teaches away from using the complex and exacting solder bump/circuit board contacts attachment method to

couple the heat sink to the die. Instead, Haley notes that that the heat sink is attached to the die with an adhesive (101) and (102) distinct from the solder bumps (107). See Col. 2 lines 66-67. Indeed, Haley claims that it is an inventive step to mount the heat sink to the die prior to attaching the die to the circuit board so that the earlier step, distinct in its method and materials, can aid in the latter, solder bump mounting step. See Col. 3 lines 17-25. There is no suggestion in either reference to use certain materials from one element as the material used to form a distinct element. Haley therefore teaches away from using tin and lead solder bumps to increase the bond strength between Hawthorne et al.'s semiconductor chip and heat slug. Furthermore, there is no suggestion in Hawthorne et al. to use solder bumps such as those disclosed in Haley to increase the bond strength of the die attachment to its heat slug.

Claim 13 should also be allowable at least for the reason that there is no motivation to combine said references. Examiner states that an "ordinary artisan would have been motivated to modify Hawthorne et al. in the manner described above for at least the purpose of decreasing moisture inside of the package." Hawthorne et al., however, never suggests any need for using tooling holes such as those disclosed in Haley to prevent moisture, and Haley's tooling holes are disclosed as being designed to aid in the optical alignment of the die in the process of locating the die on the circuit board. See Haley, col. 3 lines 25-40. Further, Hawthorne et al. discloses no suggestion of a use for tooling holes for either purpose.

With regard to Independent Claim 19, as amended, Applicants respectfully traverse the rejections due to a lack of motivation to combine the cited references. Claim 19, as amended, recites in pertinent part, "a solder film that bonds the heat slug to the backside of the semiconductor chip wherein the top portion of the heat slug contacts the conductive solder film and the side end portions of the heat slug are attached to the substrate by an adhesive, and wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that

contacts the solder film." As noted above with respect to Claim 3, Hawthorne et al. discloses no flexible substrate coupled directly to the bottom of the die from which Maheshwari et al.'s balance plate would counteract the force and minimize warpage. See Hawthorne et al. Col. 3 lines 62-64 and Fig 3. Therefore, for at least the reasons stated above with respect to the metal layer of Claim 3, there is no teaching or suggestion of a motivation to combine the said references with respect to a semiconductor chip having "a solder film that bonds the heat slug to the backside of the semiconductor chip wherein the top portion of the heat slug contacts the conductive solder film and the side end portions of the heat slug are attached to the substrate by an adhesive, and wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that contacts the solder film", as recited in Claim 19. Thus, Claim 19 is patentable over Hawthorne et al. in light of Maheshwari et al.

Claims 18 and 20 depend from Claim 19 and should be allowable at least by virtue of their dependency from Claim 19.

Claim 15 depends from Claim 14 and is allowable for at least the same reason.

For the above reasons, Applicants request reconsideration and withdrawal of the rejection under 35 U.S.C. 103.

CONCLUSION

Claims 1-20 were pending in the application. Claims 1 and 16 have been cancelled. Applicants have rewritten claims 3 and 19 in independent form and submit that the scope of these claims is not changed by virtue of being rewritten in independent form. Applicants submit that Claims 2-15 and 17-20 are allowable and therefore request that the Examiner issue a Notice of Allowability for Claims 2-15 and 17-20. If there are any questions or if

other than allowance is contemplated for any pending claim, please contact Applicant's attorney at (415) 217-6000 (x6017) or at pwoo@skjerven.com.

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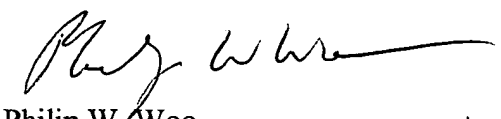
Respectfully submitted,



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ATTACHMENT A

Claims 2, 3, 5-8, 10, 11, 13, 14, 17-20 have been amended as follows. Underlines indicate additions and brackets indicate deletions.

Please cancel Claim 1 without prejudice or disclaimer.

2. The semiconductor chip package of claim [1] **3**, wherein the solder film includes one selected from a group consisting of Pb, Sn, Ag, In, and Bi.

3. (Twice Amended) [The] **A** semiconductor chip package [of claim 1] **comprising:**

a substrate having a plurality of bonding pads;

a semiconductor chip having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;

a heat slug bonded to a backside of the semiconductor chip; and

a solder film directly attached to the heat slug thereby bonding the heat slug to the backside of the semiconductor chip, wherein the backside of the semiconductor chip includes a metal layer formed thereon for strengthening adhesion between the semiconductor chip and the solder film.

5. (Amended) The semiconductor chip package of claim [1] **3**, wherein a space between the semiconductor chip and the substrate is filled with an underfilling material.

6. (Twice Amended) The semiconductor chip package of claim [1] **3**, wherein the solder film has a size equal to or larger than a size of the semiconductor chip.

7. (Amended) The semiconductor chip package of claim [1] **3**, wherein the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW.

8. (Amended) The semiconductor chip package of claim [1] **3**, wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that contacts the solder film.

10. (Twice Amended) The semiconductor chip package of claim [1] **3**, wherein the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded.

11. (Twice Amended) The semiconductor chip package of claim [1] **3**, wherein the heat slug is shaped such that a portion of the heat slug is attached to the substrate by an adhesive.

13. (Amended) The semiconductor chip package of claim [1] **3**, wherein a plurality of throughholes are formed on the heat slug.

14. (Twice Amended) A method of fabricating a semiconductor chip package, comprising:

preparing the semiconductor chip having a plurality of conductive bumps on a front surface of the semiconductor chip **and a metal layer on a backside of the semiconductor chip**;

bonding a heat slug on [a] **the** backside of the semiconductor chip using a solder film; and

attaching the semiconductor chip on a substrate such that the conductive bumps of the semiconductor chip contact a plurality of bonding pads on the substrate **wherein the metal layer on the backside of the semiconductor chip strengthens adhesion between the semiconductor chip and the solder film**.

Please cancel Claim 16 without prejudice or disclaimer.

17. The semiconductor chip package of claim [16] **19**, wherein the solder film has a size equal to or larger than a size of the semiconductor chip.

18. The semiconductor chip package of claim [16] **19**, wherein the heat slug is formed of a material selected from a group consisting of Cu, Al, and CuW.

19. (Amended) [The] **A** semiconductor chip package [of claim 16,] **comprising:**

a substrate having a plurality of bonding pads;

a semiconductor chip having a plurality of conductive bumps on a front side thereof, the conductive bumps contacting the bonding pads;

a heat slug bonded to the semiconductor chip, the heat slug comprising a top portion, side standing portions bent from the top portions, and side end portions bent again from the side standing portions; and

a solder film that bonds the heat slug to the backside of the semiconductor chip wherein the top portion of the heat slug contacts the conductive solder film and the side end portions of the heat slug are attached to the substrate by an adhesive, and wherein the heat slug comprises an adhesion layer formed on a surface of the heat slug that contacts the solder film.

20. (Previously Amended) The semiconductor chip package of claim [16] **19**, wherein the heat slug is coated with an anodizing layer on a surface of the heat slug that is opposite to another surface of the heat slug, on which the semiconductor chip is bonded.